Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)

2. (currently amended) The packet communication apparatus according to ~~claim 1~~claim 15, wherein said buffer control unit selects one of a plurality of first data ~~portions included~~ blocks stored in said plurality of ~~storing units~~ registers, ~~copies the one from said storing unit, and outputs the one to~~ and transfers a copy of the selected first data block to said ~~port buffer~~one of ingress buffers.

3. (currently amended) The packet communication apparatus according to ~~claim 1~~claim 15, wherein ~~when said scheduler permits output of said data portion to said predetermined~~ said scheduler sets up a path between said ingress buffer and said specified output ~~port, said data portion and~~ port when said acknowledge signal is issued, whereby said ~~packet~~ data block and said remaining portion subsequent to ~~said data portion~~ the first data block are transferred to said ~~predetermined~~ specified output port via ~~a switched~~ the path.

4. (currently amended) The packet communication apparatus according to ~~claim 1~~claim 15, wherein each of said ingress ~~interface~~ interfaces has a plurality of selectors of the same number as that of said ~~ingress buffers~~pairs of queue buffer and register, and

each of said selector selects either said ~~packet~~ first data ~~portion other than said data portion of said ingress buffer~~ block in the register or said ~~data~~ remaining portion in ~~said storing unit corresponding to said ingress~~ said queue buffer and outputs the selected one to ~~the switch~~said ingress buffer.

5. (currently amended) The packet communication apparatus according to claim 4, wherein

each of said ingress interfaces further comprising a packet processing unit for converting each of received packets into a plurality of internal cells each including said routing information,

said register stores a data block including at least a first cell, and said ~~ingress~~ queue buffer stores a plurality of subsequent cells ~~of said packet data~~ and a last cell in a string format~~,~~

~~said packet data includes a first cell, a subsequent cell and a last cell, said data portion is said first cell or said packet data including said first cell, said switch has counters corresponding to said output ports, said data portion is passed via a path switched by said switch and monitored at said output port, and the total value of cells of said packet data is stored in said counter~~.

6. (currently amended) The packet communication apparatus according to claim 5, wherein

said switch unit has a plurality of counters corresponding to said output ports each for storing, as an initial counter value, a total number of internal cells belonging to the same packet to be monitored at the output port,

said counter value is decremented each time said subsequent cell is monitored at said output port ~~for the total value, said total value is decremented~~ and, when said counter value becomes equal to or lower than a predetermined value, release of ~~said~~ the output port is notified to said buffer control unit.

7. (currently amended) The packet communication apparatus according to ~~claim 1~~claim 15, wherein each of said ingress ~~interface~~ interfaces is provided with a high-priority ~~ingress buffer, a storing unit,~~ pair of a queue buffer and a register and a low-priority ~~ingress buffer,~~ pair of a queue buffer and a ~~storing unit~~register, and ~~when said plurality of cells stored in said ingress buffer and storing unit are transferred, priorities are assigned~~said buffer control unit preferentially selects the high-priority pair if the register of the high-priority pair stores a first data block therein.

8. (currently amended) The packet communication apparatus according to ~~claim 6~~claim 5, wherein

each of said ~~cell has~~ internal cells is comprised of a cell header and cell data, ~~said~~ the cell header of each of said subsequent ~~cell has~~ cells includes an available port bit, ~~said output port monitors the status of the available port bit~~ and

said buffer control unit is notified of the release of said output port when ~~said output port detects~~ the change ~~of~~ in the status of the available port bit is detected at the output port~~, said buffer control unit is notified of said release~~.

9. (currently amended) The packet communication apparatus according to claim 8, wherein ~~said~~ the release of said output port is issued before said last cell passes the output port ~~can request~~ so that any one of said buffer control ~~unit to transmit the next~~ units can start transferring packet data toward the output port from a pair of queue buffer and register to said ingress buffer before said last cell ~~passes~~reaches the output port.

10. (currently amended) The packet communication apparatus according to ~~claim 1~~claim 15, wherein

each of said buffer control ~~unit~~ units includes a timer monitoring unit and ~~a~~ an acknowledge receiving unit for receiving an acknowledge signal from said switch unit, and

said buffer control unit selects said one of the other pairs of queue buffer and register when no acknowledge signal is received by said acknowledge receiving unit within a predetermined period of time measured by said timer monitoring unit after

said first data ~~portion is transmitted~~ block was output from said ~~storing unit, through monitoring by said timer monitoring unit whether said acknowledge signal is received or not within the predetermined period of time, said buffer control unit determines whether or not said scheduler permits the output of said data portion to the predetermined output port~~register.

11. (currently amended) The packet communication apparatus according to claim 4, wherein

each of said buffer control ~~unit~~ units has ~~a~~ an acknowledge receiving unit for receiving an acknowledge signal from said switch unit, and

when said acknowledge receiving unit detects that the ~~output of said data portion~~ packet transfer to said specified output port is permitted, said buffer control unit ~~selects said packet data portion other than said data portion of said ingress buffers~~ transfers the remaining portion stored in the selected queue buffer to said ingress buffer, and when said receiving unit detects that the ~~output of said data portion~~ packet transfer to said specified output port is not permitted, said buffer control unit selects ~~any~~ one of ~~said data portion of the plurality of said storing units and transmits one data portion to said switch~~the other pairs of queue buffer and register to output a new first data block to said ingress buffer.

12. (currently amended) A packet data transfer controlling method ~~using~~ in a packet communication apparatus, said apparatus having:

~~an ingress interface for inputting plural packet data;~~

a switch unit having a scheduler for ~~switching paths of the~~ scheduling packet ~~data, having~~ transfer between a plurality of input ~~ports,~~ ports and a plurality of output ~~ports, and a scheduler; and~~ports;

a plurality of ingress interfaces each coupled to one of said input ports for selectively transferring packets received from an input line to said switch unit; and

~~an~~ a plurality of egress ~~interface~~ interfaces each coupled to one of said output ports for transmitting ~~said packet data transferred via said switched path~~packets received from said switch unit to an output line,

wherein each of said ingress ~~interface~~ interfaces ~~having~~ has a plurality of pairs of a first storing ~~units, a plurality of~~ unit and a second storing ~~units corresponding to the plurality of first storing units~~unit, and a control unit for ~~controlling~~ selecting one of said ~~first and second storing units~~pairs, and said switch unit having a plurality of third storing units each associated with one of said input ports ~~having the corresponding plurality of third storing units~~so as to temporarily store packet data transferred from one of said ingress interfaces to the input port,

said method comprising the steps of:

~~storing~~ storing, by each of said ingress interfaces, packet data received from said input line in one of said first storing ~~unit~~ units, selectively and ~~transferring~~ shifting a first data portion including destination information of ~~said~~ the packet data from the first storing unit to one of said second storing ~~unit~~units, which is paired with the first storing unit;

~~receiving said~~ controlling, by each of said control units, one of said second storing units so as to transfer the first data portion ~~output from said second storing unit by~~ to one of said third storing ~~unit~~units, but leaving the same data in the second storing unit;

~~selecting~~ selecting, by said scheduler, at least one of said third storing units that stores the first data portion ~~by said scheduler, and outputting said selected~~ allowed to be transferred to one of said output ports;

controlling, by each of said control units, in response to a predetermined control signal from said scheduler, one of said first storing units, which is paired with said second storing unit from which said first data portion has been transferred, so as to transfer a remaining portion of the packet data to one of said third storing units selected by said scheduler;

transferring, by said switch unit, the first data portion and remaining portion output from said selected third storing unit to ~~a predetermined~~ one of said output ~~port~~ports specified by the destination information of the first data portion; and

~~when said data portion is not selected for said predetermined output portion by said scheduler, discarding said data portion by said third storing unit and, in response to an output request further issued from said control unit, transmitting said data portion to said third storing unit by one of said plurality of second storing units~~controlling, by each of said control units that could not receive said predetermined control signal, another of said second storing units so as to transfer

the first data portion to one of said third storing units, thereby to replace the previous first data portion with the new first data portion in the third storing unit.

13. (currently amended) The packet data controlling method according to claim 12, wherein

~~said packet data includes a first cell, a subsequent cell and a last cell,~~ each of said first storing ~~unit is an input queue buffer for storing~~ units receives said packet ~~data,~~ data as a string of fixed length cells comprising a first cell, at least one subsequent cell and a last cell, and each of said second storing ~~unit is a storing buffer for storing said~~ units receives a data ~~portion~~ block including said first cell as said first data portion from one of said input queue buffers, and said scheduler selects at least one of said third storing ~~unit is a port buffer for storing said data portion including said~~ to allow data to transfer to one of said output ports by referring to header information of first ~~cell~~cells stored in the third storing units.

14. (currently amended) The packet data transfer controlling method according to claim 12, ~~wherein in said step of transmitting, when said data portion is not selected by said scheduler, said third storing unit discards said data portion, and~~ further comprising the steps of:

monitoring output data at each of said output ports to detect completion of data transfer for a packet from one of said third storing units to the output port; and

notifying each of said control units of a port identifier indicating an available output port when the completion of data transfer to the output port was detected;

wherein each of said control ~~unit~~ units selects one of said ~~plurality of~~ second storing units ~~and outputs~~ which has failed to receive said predetermined control signal, after confirming from the notification that an output port to be used becomes available, thereby to transfer said first data portion~~, and said control unit determines again whether or not said data portion is able to be transmitted to said predetermined output port by said scheduler~~ to said third storing unit again.

15. (new) A packet communication apparatus comprising:

a switch unit having a scheduler for scheduling packet transfer between a plurality of input ports and a plurality of output ports, and a plurality of ingress buffers each connected to one of said input ports;

a plurality of ingress interfaces each connected to one of said ingress buffers for selectively transferring packets received from an input line to the ingress buffer; and

a plurality of egress interfaces each connected to one of said output ports for transmitting packets received from said switch unit to an output line;

wherein each of said ingress interfaces has plural pairs of queue buffers for storing packet data and a register capable of retransmitting stored packet data, and a buffer control unit for selecting one of said pairs of queue buffers to output stored packet data, the register of the selected pair storing a first data block including

header information of a packet received from one of said input lines and routing information for specifying one of said output ports, the queue buffer of the selected pair storing the remaining portion of the received packet,

wherein said buffer control unit controls the selected register to output said first data block to one of said ingress buffers,

wherein said scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer, and

wherein the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving said acknowledge signal, and otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of said ingress buffers, thereby to replace the previous first data block with the new first data block in the ingress buffer.